

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings of claims in the application:

**Listing of Claims:**

1                    1. (original) In a memory controller, for use in a programmable logic device for  
2 connection to an external memory device, a method of performing a prefetch operation, the  
3 method comprising:

4                    testing whether a present read access request is such that there is a high  
5 probability that said present read access request relates to configuration data for said  
6 programmable logic device; and

7                    performing a prefetch operation only if it is determined that there is a high  
8 probability that said present read access request relates to configuration data for said  
9 programmable logic device.

1                    2. (original) A method as claimed in claim 1, wherein the step of testing  
2 whether a present read access request is such that there is a high probability that said present read  
3 access request relates to configuration data for said programmable logic device  
4 comprises:

5                    determining whether the present read access request relates to a burst type from a  
6 predetermined group of suitable burst types, selected from the possible burst types.

1                    3. (original) A method as claimed in claim 2, wherein the predetermined group  
2 of suitable burst types comprises defined length accesses.

1                    4. (original) A method as claimed in claim 1, further comprising, if it is  
2 determined that a prefetch operation is to be performed:

3                    when the present read access request is completed, testing whether a read buffer  
4 contains an amount of unused space exceeding a predetermined threshold; and

5 performing the prefetch operation only if it determined that the read buffer  
6 contains an amount of unused space exceeding a predetermined threshold.

1 5. (original) A method as claimed in claim 4, further comprising prefetching a  
2 predetermined amount of data.

1 6. (original) A method as claimed in claim 5, wherein said predetermined  
2 threshold for said amount of unused space in the read buffer corresponds to said predetermined  
3 amount of data.

1 7. (original) A method as claimed in claim 5, further comprising, after  
2 prefetching said predetermined amount of data:  
3 testing whether said read buffer still contains an amount of unused space  
4 exceeding said predetermined threshold; and  
5 continuing a prefetch operation only if it determined that the read buffer still  
6 contains an amount of unused space exceeding said predetermined threshold.

1 8. (original) A method as claimed in claim 7, further comprising prefetching a  
2 further predetermined amount of data.

1 9. (original) A method as claimed in claim 2, further comprising, if a further  
2 read access request is received while a prefetch operation is in progress:  
3 determining whether said further read access request relates to a burst type from  
4 said predetermined group of suitable burst types; and  
5 terminating said prefetch operation if said further read access request does not  
6 relate to a burst type from said predetermined group of suitable burst types.

1 10. (original) A method as claimed in claim 9, further comprising, if a further  
2 read access request is received while a prefetch operation is in progress, and if said further read  
3 access request does not relate to a burst type from said predetermined group of  
4 suitable burst types:

5 flushing prefetched data from a read buffer, and subsequently performing the  
6 operation requested in said further read access request.

1 11. (original) A method as claimed in claim 9, further comprising continuing  
2 said prefetch operation, and returning prefetched data to a requesting device, only if a start  
3 address of said further read access request corresponds to a start address of said prefetch  
4 operation which is in progress.

1 12. (original) A programmable logic device, comprising:  
2 a configuration memory, for storing configuration data; and  
3 a memory controller, for connection to an external memory device, wherein, when  
4 said memory controller receives a present read access request, said memory controller retrieves  
5 the data requested in said present read access request, and determines whether said present read  
6 access request is such that there is a high probability that said present read access request relates  
7 to configuration data for said programmable logic device; and  
8 said memory controller performs a prefetch operation after completing retrieval of  
9 the data requested in said present read access request only if it is determined that there is a high  
10 probability that said present read access request relates to configuration data for said  
11 programmable logic device.

1 13. (original) An electronic system, comprising a programmable logic device  
2 and an external memory device, wherein said programmable logic device comprises:  
3 a configuration memory, for storing configuration data; and  
4 a memory controller, for connection to said external memory device, wherein,  
5 when said memory controller receives a present read access request, said memory controller  
6 retrieves the data requested in said present read access request, and determines whether said  
7 present read access request is such that there is a high probability that said present read access  
8 request relates to configuration data for said programmable logic device; and  
9 said memory controller performs a prefetch operation after completing retrieval of  
10 the data requested in said present read access request only if it is determined that there is a high

11 probability that said present read access request relates to configuration data for said  
12 programmable logic device.

1 14. (original) An electronic system as claimed in claim 13, wherein said external  
2 memory device comprises a flash memory device.

1 15. (original) An electronic system as claimed in claim 13, wherein said external  
2 memory device comprises a SRAM device.

1 16. (canceled)

1 17. (new) A programmable logic device as claimed in claim 12, wherein said  
2 memory controller determines whether said present read access request is in the form of a  
3 defined length burst.

1 18. (new) A programmable logic device as claimed in claim 12, wherein said  
2 memory controller performs a prefetch operation after completing retrieval of the data requested  
3 in said present read access request only if it is determined that a read buffer contains an amount  
4 of unused space exceeding a predetermined threshold.

1 19. (new) A programmable logic device as claimed in claim 12 wherein, if a  
2 further read access request is received while a prefetch operation is in progress, said memory  
3 controller returns prefetched data to a requesting device if:

4 the further read access request relates to a defined length burst;

5 the further read access request corresponds to a same chip select of said prefetch  
6 operation which is in progress; and

7 the start address of said further read access request corresponds to a start address  
8 of said prefetch operation which is in progress.

1 20. (new) An electronic system as claimed in claim 13, wherein said memory  
2 controller determines whether said present read access request is in the form of a defined length  
3 burst.

1                    21. (new)      An electronic system as claimed in claim 13, wherein said memory  
2 controller performs a prefetch operation after completing retrieval of the data requested in said  
3 present read access request only if it is determined that that buffer space is available.

1                    22. (new)      An electronic system as claimed in claim 13, wherein, if a further  
2 read access request is received while a prefetch operation is in progress, said memory controller  
3 returns prefetched data to a requesting device if:

4                    the further read access request relates to a defined length burst;

5                    the further read access request corresponds to a same chip select of said prefetch  
6 operation which is in progress; and

7                    the start address of said further read access request corresponds to a start address  
8 of said prefetch operation which is in progress.